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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,611	09/18/2003	KokHoe Chia	STL11343	4044

7590 10/21/2005

Seagate Technology LLC
1280 Disc Drive
Shakopee, MN 55379

EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,611	CHIA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 18 September 2003 was fully considered by the examiner.

Drawings

2. The drawings submitted on 18 September 2003 are acceptable to the Examiner.

Claim Objections

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claim 17 has been renumbered as claim 14.

4. Claims 6-7 and 14 are objected to because of the following informalities:

As for claim 6, it is unclear how "new data cache parameters" as recited in this claim can be stored without first claiming "data cache parameters" (i.e. "original" or "old" parameters).

As for claim 14, it is unclear how the "new data cache parameters" stored became "new" from the original "data cache parameters" as claimed in claim 9.

Claim 7 is objected to for further limiting claim 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 and 9 recite the limitation of "reallocating" in lines seven and thirteen of these claims respectively. There is insufficient antecedent basis for this limitation in the claims, as both claims fail to previously set forth "allocating", hence the unused memory space recited in these claims can not be reallocated. The claims will further be treated on their merits by replacing "reallocating" with "allocating".

Claims 2-8 and 10-14 further limit claims 1 and 9 respectively, therefore they too are rejected under 35 USC § 112.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchimoto et al. (hereinafter Tsuchimoto) US Patent 6,336,202 B1.

As for claim 1, Tsuchimoto teaches a method of managing a buffer random access memory, the buffer random access memory having a first portion reserved for a defect table and a second portion reserved for data caching, the method comprising (referring to Fig. 1, the controller (element 5) is comprised of a buffer RAM

(element 14). The RAM further includes a section of memory, which is used to store a defect table (col. 3, lines 45-50 – the controller reads the defect map (table) from a disk and writes it to the RAM), and the remaining section is used for data caching (col. 3, lines 20-25 – data to be written or read is cached in the RAM)):

determining actual memory space of the first portion of the buffer random access memory occupied by the defect table to identify unused memory space of the first portion (as noted above, col. 3 lines 20-25 and 45-50 demonstrate how the RAM is divided between the defect table and data caching. The controller as illustrated in Fig. 1 must inherently make a determination which data in the RAM is the defect table and which area in the RAM is for data caching in order for Tsuchimoto's system to work); and

allocating the unused memory space of the first portion of the buffer random access memory for use in data caching (the remaining memory area in the RAM, not being used to store the variable sized defect table can now be used (i.e. allocated) for data caching purposes. Referring to col. 5, lines 57-67, Tsuchimoto aims at minimizing the size of the defect map so that it occupies a minimal amount of the RAM in the controller. The remaining area of the RAM is now allocated for data caching purposes as described in col. 3, lines 20-25).

As for claim 8, Tsuchimoto teaches a controller configured to implement the method of claim 1 (referring again to Fig. 1, the controller (element 5) controls an MPU (element 12) and an HDC (element 11), which are used to executes control over the data storage system (col. 3, lines 18-25)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchimoto as applied to claim 1, and in further view of Beng Sim et al. (hereinafter Beng Sim) US PG Publication 2002/0108072 A1.

As for claim 2, though Tsuchimoto teaches determining the actual memory space of the first potion of the buffer random access memory, he fails to specifically teach obtaining information on a total number of defects identified on a storage media, nor does he teach determining, by calculating, the memory space occupied in the first part of the memory by the defect table based upon the number of defects identified.

Beng Sim however teaches a method for adaptive storage and caching of a defect table in which a defect table (Fig. 4, element 430) is created and stored on a storage medium (element 410) and subsequently transferred and stored in a volatile memory (element 450) - Paragraph 0048, lines 1-12.

More specifically, Beng Sim teaches obtaining information on a total number of defects identified on a storage media, and calculating the actual memory

space of the first portion of the buffer random access memory occupied by the defect table based upon the total number of defects identified on the storage media (paragraph 0063, lines 1-9 – the volatile memory is partitioned into one or more segments based on the quantity of defects of the mass storage device (i.e. number of defects is identified on the media), hence amount of memory needed to store the table referencing the defects inherently must calculate the table's size into order to appropriately allocate memory for its storage).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Tsuchimoto to further include Beng Sim's method for adaptive storage and caching to his data storage system. By doing so, Tsuchimoto could exploit the advantages of using a defect table that is fully adaptable and dynamic in size, capacity and length which would help improve the system's efficiency by reducing the seek time between regions of data and the defect table as taught by Beng Sim (paragraph 0014, lines 1-17).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchimoto and in further view of Tzelnic et al. (hereinafter Tzelnic) US Patent 5,948,062.

As for claim 9, Tsuchimoto teaches a mass storage device comprising:

a storage media (Fig. 1, element 1) storing a defect table (col. 3, lines 45-47 – the controller reads the defect table that is presently stored on the disk);

a buffer random access memory having a first portion reserved for the defect table and a second portion reserved for data caching (referring to Fig. 1, the controller (element 5) is comprised of a buffer RAM (element 14)). The RAM further includes a section of memory, which is used to store a defect table (col. 3, lines 45-50 – the controller reads the defect map from a disk and writes it to the RAM), and the remaining section is used for data caching (col. 3, lines 20-25 – data to be written on read is cached in the RAM), the defect table being uploaded into the buffer random access memory from the storage media (col. 3, lines 45-50, the defect table is read from the disk and written to the RAM); and

a controller operable coupled to the storage media (Fig. 1, controller (element 5) is connected to the disk), and to the buffer random access memory (the controller comprises the RAM therefore they are inherently coupled to one another), the controller configured to implement the steps of:

determining actual memory space of the first portion of the buffer random access memory occupied by the defect table to identify unused memory space of the first portion (as noted above, col. 3 lines 20-25 and 45-50 demonstrate how the RAM is divided between the defect table and data caching. The controller as illustrated in Fig. 1 must inherently make a determination which data in the RAM is the defect table and which area in the RAM is for data caching in order for Tsuchimoto's system to work); and

allocating the unused memory space of the first portion of the buffer random access memory for use in data caching (the remaining memory area

in the RAM, not being used to store the variable sized defect table can now be used (i.e. allocated) for data caching purposes. Referring to col. 5, lines 57-67, Tsuchimoto aims at minimizing the size of the defect map so that it occupies a minimal amount of the RAM in the controller. The remaining area of the RAM is inherently now allocated for data caching purposes as described in col. 3, lines 20-25).

Tsuchimoto however fails to teach storing data cache parameters in a storage media, nor uploading the data cache parameters from the storage media, into the buffer random access memory as claimed by applicant.

Tzelnic however teaches a file server using a cached disk array with shared read-write file access, which includes a storage media (Fig. 14, element 215), which stores parameters (file attributes – element 222), which are loaded into the buffer cache (element 213). The file attributes contain attribute information on the file data contained in the buffer hence are "data cache parameters" – col. 16, line 57 through col. 17 line 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Tsuchimoto to further include Tzelnic's system in order to avoid possibility of losing critical file data and file attribute information during a system crash (as one of ordinary skill in the art recognizes that crashes are always of concern to system's such as the Tsuchimoto's data storage system). By storing the critical file data and file attribute information in both the cache and the storage media and disclosed by Tzelnic, Tsuchimoto would benefit by being able to retrieve newly stored information from the

disk, preventing data loss from the buffer during a system crash as taught by Tzelnic (col. 16, lines 27-39).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Tsuchimoto and Tzelnic as applied to claim 9 above, and in further view of Beng Sim.

As for claim 10, though Tsuchimoto teaches determining the actual memory space of the first potion of the buffer random access memory, he fails to specifically teach obtaining information on a total number of defects identified on a storage media, nor does he teach determining, by calculating, the memory space occupied in the first part of the memory by the defect table based upon the number of defects identified.

Beng Sim however teaches a method for adaptive storage and caching of a defect table in which a defect table (Fig. 4, element 430) is created and stored on a storage medium (element 410) and subsequently transferred and stored in a volatile memory (element 450) - Paragraph 0048, lines 1-12.

More specifically, Beng Sim teaches obtaining information on a total number of defects identified on a storage media, and calculating the actual memory space of the first portion of the buffer random access memory occupied by the defect table based upon the total number of defects identified on the storage media (paragraph 0063, lines 1-9 – the volatile memory is partitioned into one or more segments based on the quantity of defects of the mass storage device (i.e. number of

defects is identified on the media), hence amount of memory needed to store the table referencing the defects inherently must calculate the table's size into order to appropriately allocate memory for its storage).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Tsuchimoto to further include Beng Sim's method for adaptive storage and caching to his data storage system. By doing so, Tsuchimoto could exploit the advantages of using a defect table that is fully adaptable and dynamic in size, capacity and length which would help improve the system's efficiency by reducing the seek time between regions of data and the defect table as taught by Beng Sim (paragraph 0014, lines 1-17).

Allowable Subject Matter

10. Claims 3-7 and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. More specifically, these claims cannot be deemed allowable until they are rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

11. The following is a statement of reasons for the indication of allowable subject matter:

As for claims 3 and 11, The combined teachings of Tsuchimoto, Beng Sim and Tzelnic fails to teach swapping locations of the defect table and unused memory space such that the unused memory space is closest to the second portion of the buffer random access memory for caching.

Claims 4-7 and 12-14 further limit claims 3 and 11 respectively therefore they too are deemed allowable.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

MANO PADMANABHAN 10/13/05
SUPERVISORY PATENT EXAMINER